# Reese Kuper

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## EDUCATION

**Masters** – University of Illinois at Urbana-Champaign (3.96/4.00) 2021 - 2023
*Department of Electrical and Computer Engineering*
Focus: Computer Architecture

**Bachelors** – University of Wisconsin-Madison (3.89/4.00) 2017 - 2021
*Degrees in Computer Engineering and Computer Science*

### Relevant Coursework

- Parallel Computer Architecture
- Computer Microarchitecture
- Artificial Intelligence
- Advanced Computer Architecture
- Digital System Design & Synthesis
- Algorithms
- Memory and Storage Systems
- Operating Systems
- System-on-Chip Design

## EXPERIENCE

**Intel Inc.** September 2022 - September 2023
Graduate Research Intern – On-Chip Accelerators *Remote*

- Conducted performance analysis on DSA – an on-chip accelerator found on Sapphire Rapids and later Xeon processors.
- Explored use cases for DSA to take advantage of cache pollution mitigation and higher throughput for memory operations.
- Submitted patents for improving memory deduplication techniques using DSA.
- Prepared and Presented a tutorial for Intel's on-chip accelerators at ISCA 2023.

**Samsung Semiconductor Inc.** Summer 2022
Graduate Research Intern – Memory Systems Laboratory *San Jose, CA*

- Investigated the effectiveness of an L1 cache in a CXL device for DLRM offloading.
- Built a functional cache simulator to evaluate both hit rates and cache occupancy rates of real DLRM memory traces.
- Analyzed the characteristics of real DLRM data for locality patterns to aid in the design of the memory system.
- Simulated DRAM and cache designs via Ramulator to obtain bandwidth, hit rate, and other metrics used in analysis.

**Arm Ltd.** Summer 2021
Hardware Engineering Intern – CPU Memory System Verification *Austin, TX*

- Debugged failing signatures for the CPU memory system testbench.
- Implemented new statistical coverage (SCOV) workflow:
  - Used scoreboard listener functions to implement SCOV events for assessing stimulus coverage.
  - Coded macro for ease of adding additional SCOV events within the UVM testbench.
  - Developed Python script to parse generated simulation log files during regression tests to send to a MySQL database.

**Arm Ltd.** Summer 2020
Hardware Engineering Intern – Systems Interconnect Verification *Austin, TX*

- Developed internal Python tool to analyze the use of all plusargs within the UVM testbenches.
- Fixed UVM register definition auto-generation for more flexible RAL models.
- Programmed module for modeling transactions between a master device to interconnect return nodes in SystemC.
- Formally verified round robin and LSB priority arbiters using System Verilog assertions.

**Qualcomm Inc.** Summer 2020
Software Engineering Intern – Linux Kernel Memory System *San Diego, CA*

- Improved kernel ION allocation memory speeds by around 10%.
- Analyzed the efficiency of IOVA's use of caching and compared it with MMAP's gap searching RBTree.
- Created internal Python tool for parsing Linux RAM dump binaries.
- Worked towards shifting mmap allocations to use the mempool API.

## PROJECTS

### Relevant Projects and Research

- Investigated finer-grained GPU scheduling for improved GPU utilization in machine learning workloads.
- Self-balancing Segway written in Verilog for a DE0-Nano FPGA board.
- Synthesized a 5-stage pipelined CPU and a dataflow processor written in Verilog.
- Implemented prefetcher designs and age matrix issueing schemes for BOOM RISC-V processor on an FPGA.

## SKILLS

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|---|---|
| **Hardware Description and Programming Languages** | System Verilog, C/C++, Python, Bash Scripting, MySQL |
| **Development and Software Tools** | Vivado, Vivado HLS, ModelSim, Quartus, Vim, Git |

## PUBLICATIONS AND CONFERENCES

- **CXL≠NUMA: Device-Specific Characteristics and Effective Use of True CXL Memory**
  Y. Sun, Y. Yuan, Z. Yu, C. Song, **R. Kuper**, J. Huang, H. Ji, S. Agarwal, J. Lou, I. Jeong, R. Wang, J. H. Ahn, T. Xu, N. S. Kim
  International Symposium on Microarchitecture (**MICRO**), 2023
- **On-chip Accelerators in 4th Gen Intel® Xeon® Scalable Processors: Features, Performance, Use Cases, and Future!**
  **R. Kuper**, I. Jeong, Y. Yuan, J. Hu, R. Wang, N. Ranganathan, N. S. Kim
  [TUTORIAL] International Symposium on Computer Architecture (**ISCA**), 2023
- **A Quantitative Analysis of Data Streaming Accelerator in Intel Sapphire Rapids Xeon Scalable Processors**
  **R. Kuper**, I. Jeong, Y. Yuan, J. Hu, R. Wang, N. Ranganathan, N. S. Kim
  Open-access ePrint Archive (**arXiv**), 2023
- **STYX: Exploiting SmartNIC Capability to Reduce Datacenter Memory Tax**
  H. Ji, Y. Sun, M. Mansi, Y. Yuan, J. Huang, **R. Kuper**, M. Swift, N. S. Kim
  The USENIX Annual Technical Conference (**ATC**), 2023
- **Demystifying CXL Memory with Genuine CXL-Ready Systems and Devices**
  Y. Sun, Y. Yuan, Z. Yu, **R. Kuper**, I. Jeong, R. Wang, N. S. Kim
  Open-access ePrint Archive (**arXiv**), 2023
- **Improving GPU Utilization in ML Workloads Through Finer-Grained Synchronization**
  **R. Kuper**, S. Pati, M. Sinclair
  Young Architect Workshop (**YArch**), 2021